

SEMICONDUCTOR PACKAGE WITH PERFORATED SUBSTRATE

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Background

The invention relates to a semiconductor package and to a substrate for a semiconductor package, and to methods for assembling the substrate and semiconductor package.

10 The performance and reliability of semiconductor packages is limited by stresses within the package which occur during the manufacturing process.

JP 3283453 discloses a semiconductor package which includes a moisture absorbing material bonded to the rear of the die pad. KR 2002064592-A discloses a semiconductor package which includes a vent hole. These packages are not very reliable and many packages are discarded after manufacturing.

15 For these and other reasons, there is a need for the present invention.

Summary

One aspect of the present invention provides a more reliable semiconductor package and a simple, cost-effective method for assembling such a package.

20 A semiconductor package according to one embodiment of the invention includes a substrate and a semiconductor chip which includes an active surface with a plurality of chip contact areas. The chip contact areas are electrically connected to the upper contact areas of the substrate. The substrate includes, for example, a redistribution board.

25 The substrate for a semiconductor package according to one embodiment of the invention includes a perforated sheet of core material. The core material includes an electrically insulating or dielectric material such as a plastic or a ceramic or a BT substrate.

30 The substrate also includes a plurality of upper conducting traces and upper contact pads or areas on its upper surface and a second plurality of lower conductive traces and external contact areas on its bottom surface. A plurality of conducting vias which are positioned essentially vertically through the thickness of the substrate and

electrically connect the upper conducting traces and lower conducting traces of the substrate. A plurality of vent holes or non-plated through holes is provided. A layer of solder resist covers the upper and lower surfaces of the substrate leaving the contact areas free from solder resist.

5 The non-plated through holes or vent holes are positioned essentially vertically in the substrate and penetrate the upper and lower surfaces of the substrate forming open-ended through holes. The vent holes have a diameter in one case of approximately $1\mu\text{m}$ to approximately 5mm , or more in another case, approximately $10\mu\text{m}$ to approximately 0.5mm or even more in another case, approximately $100\mu\text{m}$.

10 With the diameters of the through holes, the non-plated through holes are positioned laterally between the conducting traces and contact areas on the upper and lower surface of the substrate. The conducting paths are, therefore, not disrupted by the position of the vent holes. In one case, the vent holes are included in a standard substrate which already includes conducting traces and contacts areas in a desired
15 arrangement or design.

Analysis by the inventors has illustrated that the invention reduces stresses inside the package during the manufacturing process, and in some cases during the solder reflow process, leading to an improved reliability of the packages. This is the case even when there is moisture inside semiconductor packages.

20 With the non-plated through holes included in the substrate of the invention, moisture escapes from the core material of the substrate through the side walls of the non-plated through holes as the side walls of the vent holes include no metal or electrically conducting coating or layer. The metal electro-plated coating on the inner walls of the conducting vias is impermeable to moisture. The metal coating of the
25 conducting vias therefore prevents moisture from escaping from the core material through the center of the via. With the inclusion of the non-plated through holes in the substrate of the invention, therefore, moisture escapes from the package in a three-dimensional way.

The substrate according to one embodiment of the invention is used in a
30 semiconductor package, such as a laminate package which includes a substrate, for example, flip-chip or ball grid array packages. In one example, the chip is mounted to the substrate by the flip chip technique. Microscopic solder balls connect the chip

contact areas to the upper contact areas of the substrate. In one case, the area between the active surface of the chip and the upper surface of the substrate is underfilled by epoxy resin or underfill material. In such case, the delicate electrical connections formed by the microscopic solder balls are protected.

5 In an alternative embodiment, the chip is encapsulated by mold material. In such case, the outer surface of the chip and upper surface of the package are protected.

The plurality of vent holes are in one case laterally located towards the center of the substrate. This enables moisture in the core material at the center of the substrate to escape through the vent holes. As the vent holes are positioned in the substrate under
10 the chip and underfill material, the vent holes act as a channel for moisture relief from the underfill material and chip and from the interfaces between the chip, underfill material and substrate. The vent holes provide an efficient moisture relief path, reducing stress at the interfaces and package reliability is improved.

Alternatively, the plurality of vent holes are laterally located towards the center
15 and towards the outer edges of the substrate. With this arrangement of the vent holes when the chip is overmolded or encapsulated by, for example, mold material or plastic as moisture escapes from the mold material through the vent holes as well as from the outer surfaces. The escape of moisture from the package is therefore enhanced.

In one embodiment of the invention the non-plated through holes or vent holes
20 include solder resist. Alternatively, the vent holes are filled by solder resist. In such case, moisture more easily escapes from the package as solder resist is extremely permeable to moisture.

In an embodiment of the invention the vent holes are closed at one end by a layer of solder resist on the upper surface of the substrate. With this, the solder resist layer is
25 more easily applied to the substrate.

The arrangements of the solder resist, the underfill material or mold material does not enter the vent holes. As mold material is not permeable to moisture, the vent holes are not filled or partially filled by moisture blocking material and moisture can more easily escape from the package through the vent holes.

30 A method to assemble a substrate for a semiconductor package includes the following steps. Firstly a substrate is provided. The substrate includes a sheet of core material, a plurality of upper contact traces and upper contact pads on its upper surface,

a second plurality of lower conducting traces and external contact areas on its bottom surface and conducting vias connecting the upper conducting traces and lower conducting traces. A plurality of vent holes is then formed in the substrate.

5 In one embodiment, the upper and lower surfaces of the substrate are covered by a layer of solder resist leaving the upper and lower contact areas free from solder resist.

Alternatively, the vent holes are formed in the core material before a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and conducting vias are deposited.

10 In one case, the vent holes are formed by drilling.

A method to assemble a semiconductor package includes the following steps. A semiconductor chip comprising an active surface including a plurality of chip contact areas and a substrate as described above is provided.

15 The chip is mounted on the upper surface of a substrate according to one embodiment of the invention by microscopic solder balls between the chip contacts and upper contact areas. A solder reflow is performed. The area between the chip and the upper surface of the substrate is underfilled with epoxy resin and external contacts such as solder balls are attached to the external contact areas of the substrate.

20 In an embodiment the upper surface of the chip and substrate are covered with mold material to encapsulate the chip.

25 In one embodiment of the invention the performance and reliability of semiconductor or IC packages are improved. The non-plated through holes or vent holes provided in the substrate provide paths or channels for the free and easy emission of moisture from the package, and in one case, during the solder reflow process when the package is heated.

The size and distribution of the non-plated through holes within the substrate are chosen so that the channels and surfaces formed by the holes provide an efficient moisture relief from the package in a three-dimensional way.

30 Semiconductor packages containing the perforated substrate according to one embodiment of the invention do not suffer high vapour pressure and high moisture content in the interface between the semiconductor chip or die and the die attach or underfill material, the interface between the die attach or underfill material and the

substrate, the interface between the mold material or molding compound or plastic housing and the substrate and within the substrate. Hygroscopic stresses are reduced by use of the substrate according to one embodiment of the invention and the reliability of the packages is improved. Stresses within and warping of packages which include a perforated substrate according to one embodiment of the invention are reduced and the performance and reliability improved.

Brief Description of the Drawings

The accompanying drawings are included to provide a further understanding of the present invention and are incorporated in and constitute a part of this specification. The drawings illustrate the embodiments of the present invention and together with the description serve to explain the principles of the invention. Other embodiments of the present invention and many of the intended advantages of the present invention will be readily appreciated as they become better understood by reference to the following detailed description. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

Figure 1 illustrates a flip-chip semiconductor package including an exposed semiconductor chip.

Figure 2 illustrates a cross-sectional view of a flip-chip semiconductor package including an overmolded semiconductor chip.

Figure 3 illustrates a top view of the upper surface of the substrate of the semiconductor package of Figure 1 or Figure 2.

Figure 4 illustrates a cross-sectional view of an alternative embodiment of a flip-chip package.

Detailed Description

In the following Detailed Description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the Figure(s) being described. Because components of embodiments of the present invention can be positioned in a number of

different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Figure 1 illustrates a cross-sectional view of a semiconductor package 1 which includes an exposed semiconductor chip 2 mounted by the flip-chip technique to a redistribution board 3.

The redistribution board 3 includes a sheet of core material 5 and includes a plurality of upper conducting traces 6 and upper contact pads 7 on its upper surface and a second plurality of lower conductive traces 8 and external contact areas 9 on its bottom surface.

The redistribution board 3 also includes a plurality of essentially vertical plated via holes or conducting vias 10 which penetrate the redistribution board from the upper to lower surface. The inner surfaces of the plated via holes 10 are covered by an electrically conducting coating 11 deposited by an electro-plating technique. The upper contact pads 7 on the upper surface of the redistribution board 3 are electrically connected with an external contact area 9 on the bottom surface of the redistribution board 3 by a continuous conducting path formed by upper conductive traces 6, the conducting coating 11 of via holes 10 and the second lower conductive traces 8. A complete conducting path is not seen for every upper contact pad 7 or external contact area 9 in the cross-section of Figure 1 due to the lateral positioning of the upper contact pads 7, external contact areas 9 and conductive traces 6 and 8. The lateral positioning of the upper conducting traces 6 and upper contact pads 7 can be more clearly seen in the top view of Figure 3 which is described later.

The redistribution board 3 also includes a plurality of non-plated through holes or vent holes 4 which are positioned essentially vertically and penetrate the redistribution board from the upper to the lower surface. The inner surface of the non-plated through holes 4 does not include a metal coating. The non-plated through holes 4 are laterally positioned in the redistribution board 3 in areas which do not include conductive traces or contact areas on either the upper or lower surface. The non-plated through holes 4 and plated via holes 10 are located laterally throughout the redistribution

board 3; Some are positioned in the redistribution board 3 towards the lateral center so that they are under the chip 2 and others are positioned towards the outer edges of the redistribution board 3 so that they are laterally adjacent to the chip 2.

Solder balls 12 are attached to the external contact areas 9 to provide the
5 electrical connection from the package 1 to an external circuit board (which is not illustrated in the Figure).

The semiconductor chip 2 includes an active surface including a plurality of chip contact areas 13 and a passive surface. The chip 2 is electrically connected to the redistribution board 3 by microscopic solder balls 14 between the chip contact areas 13
10 and the upper contact pads 7 on the upper surface of the redistribution board 3.

The upper and lower surfaces of the redistribution board are coated with a layer of solder resist 15. The volume of the plated via holes 10 and non-plated through holes 4 is also filled by the solder resist layer 15. The contact pads 7, contact areas 8 and solder balls 14 are not covered by the solder resist layer 15. The area between the active
15 surface of the chip 2 and the upper surface of the redistribution board 3 is filled by underfill material 16.

The different paths by which moisture can exit the package to the environment are indicated by the arrows 17. Moisture exits the chip 2 and epoxy underfill 16 mainly downwards through the solder resist 15 located in the non-plated through holes 4 as well
20 as through the plated via holes 10 and from the outer surfaces of the chip 2 and epoxy underfill 6 which are in contact with the environment.

Moisture contained within the core material 5 of the redistribution board 3 exits mainly through the side walls of the non-plated through holes 4 and the solder resist within them. For non-plated through holes 4 located under the semiconductor chip 2,
25 the moisture exits mainly downwards. Moisture within the core material 5 also exits the redistribution board 3 from its outer surfaces.

Figure 2 illustrates a cross-sectional view of an embodiment of the invention which includes a flip-chip semiconductor package 18 including a semiconductor chip 2 which is encapsulated by mold material 19. The redistribution board of the package 18
30 is essentially the same as that of package 1 illustrated in Figure 1. Parts of the package which are similar have the same reference number and are not necessarily described again. The chip 2 and upper surface of the redistribution board 3 are covered by mold

material 19. As indicated by the arrows 17, moisture exits the mold material 19 mainly through the solder resist within the via holes 10 and non-plated through holes 4 as well as through the outer surfaces of the mold material 19 which are in contact with the environment.

5 Figure 3 illustrates a plan view of the upper surface of the redistribution board 3 of the semiconductor package 1, 18 of Figure 1 or Figure 2. Contact pads 7 are connected by conductive traces 6 to plated via holes 10. The redistribution board 3 also includes a plurality of non-plated through holes 4 which are laterally located in the redistribution board 3 between the conductive traces 6, contact pads 7 and plate via
10 holes 10. Some of the non-plated through holes 4 are located towards the center of the redistribution board 3 while others are located towards the outer edges of the redistribution board 3.

 Figure 4 illustrates a cross-sectional view of a flip-chip semiconductor package 20 including a semiconductor chip 2 according to a further embodiment of the invention.
15 The redistribution board of the package 20 is similar to that of package 1 and 18 illustrated in Figures 1 and 2. Parts of the package which are similar have the same reference number and are not described again. In this embodiment of the invention, the redistribution board 21 includes non-plated through holes or vent holes 22 which are closed at the upper surface of the redistribution board 21 by a layer of solder resist 15.
20 The vent holes 22 are not filled by solder resist.

 The invention also relates to methods to assemble a substrate and a semiconductor package.

 In the first step of the process, a redistribution board 3; 21 is provided. The redistribution board 3; 21 includes a sheet of insulating core material 5 and a plurality of
25 contact traces 6 and contact pads 7 on its upper surface, a second plurality of conducting traces 8 and external contact areas 9 on its bottom surface and conducting vias or plated via holes 10 connecting conducting traces 6 and lower conducting traces 8. A plurality of vent holes 4 are then drilled through the redistribution board 3, forming through-holes from the upper to the lower surface. The upper and lower surfaces of the redistribution
30 board 3; 21 are then covered by a layer of solder resist 15 leaving the contact areas 6 and 8 free from solder resist 15.

In one embodiment of the invention the vent holes 4 are filled with solder resist 15. In an alternative embodiment, the vent holes 22 are closed at the upper surface of the redistribution board by solder resist 15.

5 The redistribution board 3; 21 assembled using one of the above method is then used assemble a semiconductor package 1; 18; 20. A semiconductor chip 2 comprising an active surface including a plurality of chip contact areas 13 is mounted on the upper surface of the redistribution board 3; 21 by microscopic solder balls 14 between the chip contacts 13 and upper contact pads 7.

10 The package 1 then undergoes a solder reflow heat treatment. The area between the chip 2 and the upper surface of the redistribution board 3; 21 is underfilled by epoxy resin or underfill material 16. Solder balls 12 are attached to the external contacts 9 of the redistribution board 3; 21.

15 In an alternative embodiment of the method, after the semiconductor chip 2 is underfilled with underfill material 16, the upper surface of the chip 2 and redistribution board 3 are coated by mold material 19 to form an over-molded semiconductor package 18.

In an alternative method, the vent holes 4; 22 are drilled into the core material 5 of the redistribution board 3; 21 before the conductive traces 6 and 8, contact areas 7 and 9 and conducting vias 10 are deposited on the redistribution board 3; 21.

20 The semiconductor packages 1; 18; 20 are then tested, packaged and transported to the customer. The semiconductor packages are mounted to external substrates such as a printed circuit board.

25 Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.